



# Power-Aware Testing and Test Strategies for Low Power Devices

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## Power-Aware Testing and Test Strategies for Low Power Devices

Managing the power consumption of circuits and systems is now considered one of the most important challenges for the semiconductor industry. Elaborate power management strategies, such as dynamic voltage scaling, clock gating or power gating techniques, are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test, and power-aware test is therefore increasingly becoming a major consideration during design-for-test and test preparation for low power devices. This book explores existing solutions for power-aware test and design-for-test of conventional circuits and systems, and surveys test strategies and EDA solutions for testing low power devices.

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